Short-Circuit Fault Protection Strategy of Parallel Three-phase Inverters

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***Abstract*— In this paper, a five-stage fault protection scheme against the short-circuit fault for parallel high-power three-phase combined inverter to achieve high reliability is proposed. There are two control modes, Voltage Controlled Mode (VCM) and Current Controlled Mode (CCM). VCM operates under normal operation to keep constant output voltage. CCM operates under fault operation to limit the output current, which is combined with hardware current limit circuit and software current limit unit. For parallel inverter system, the output voltage recovers quickly and then switch from CCM to VCM for inverter once the short-circuit fault is recovered. However, A little time difference of switching mode between parallel inverters results in the surge circulating current, which reduces the system reliability. Thus, the pre-synchronized state is added to achieve the current sharing at any time and to achieve simultaneous mode change for each inverter. A prototype with two parallel three-phase 400kVA/50HZ inverters is built to verify the reliability of the proposed method.**

I. INTRODUCTION

High power inverter has played a key role in industry application, such as uninterruptible power supply (UPS), high-power motor drive, flexible ac transmission system (FACT), energy storage system and renewable generation [1]. With the power capacitances increasing, the parallel technique is good choice to system reliability [2]. Distributed logic control [3] and droop control has been mainly adopted because of high reliability. All units are master unit and the system can work normally if one unit fails. The droop control does not need the communication line; however, inherent trade-off exists between the power sharing accuracy and the output voltage regulation, such as frequency and magnitude offset with load changing [4]. The distributed logic control is adopted in this paper.

Most abnormal situations, such as short-circuit fault is discussed in many literature [5-11]. The fault happens at switching devices or output side of the load. This paper only focuses on the load-side protection strategy. Normally, a small overload capability of high-power inverter is designed due to the limitation of the cost. Thus, the switching devices could be damaged without any protection method when the load side is short circuit. To cut off the short-circuit fault, circuit breakers or fuses installed between inverter and loads, which is only a normal protection method for power system. There are working time requirements, such as the 20ms-100ms for micro grid application or UPS application to fault recovery [5]. For these situations, several short-circuit protection strategy were developed for inverter [6-11]. To quickly protect the switching devices, the hardware method to cut off the driver signal has fast current limit and high reliability [9], which might avoid the switching device damage. And then software method can work to get required limited current [11]. Unfortunately, no literature focus on the short-circuit protection strategy for parallel system, there are large difference between single inverter and several parallel inverters, there is the surge circulated current between each inverter at transient operation once they have a little time difference to switch mode.

In this paper, A five-stage fault protection for the short-circuit fault for high-power parallel inverters. The five stages are normal state, hysteresis controlled state, current-controlled state, pre-synchronized state and recovery state. The inverter works in VCM at normal state. Once the short-circuit fault happens, the inverter is switched into CCM, which includes hysteresis controlled state and current controlled state by hardware and software. And then, the output current is kept constant. When the fault point is cleared, the output voltage increases quickly, the parallel inverters come into pre-synchronized state to promise the synchronized time by

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parallel communication, and then, the parallel inverters go back to VCM.

This paper is organized as follows: In Section II, the system structure and short-circuit issues of parallel inverters. Section III shows the proposed fault strategy. Section IV gives the experiment results to verify the feasibility of the proposed method. The conclusion is given in Section V.

II. System Structure and Short-Circuit Issue Issues

Fig.1 shows the parallel system based on two combined three-phase inverters. The combined three-phase inverter can provide the high power and works in unbalanced load compared to the three-phase H-bridge inverter [12].The resister r is equivalent resistance of wires, saturation voltages of the switching devices and dead-time effect. L and C is the second-order filter to eliminate the high-frequency harmonic content [13]. The line-frequency transformer is injected between the output filter LC and the load to meet galvanic isolation and to reduce instantaneous short circuit current thanks to the impedance of the leakage inductance. The parallel technique is used in distributed logic control. And there is the communication signal of each other; the detailed block diagram is show in next section. The short-circuit fault is cleared by the breaker. Usually, two stage protection breakers are used according to power requirement. The first stage protection breaker clears the instantaneous short-circuit point; when the instantaneous fault current is exceed the instantaneous threshold value. There is almost not delay time, and it is called instantaneous fault in this paper. The second stage protection breaker clear the short-circuit point after designed delay time, which is called time-limited fault in this paper [11].

For testing system, the different recovery time breakers are used, Breaker T_1 and T_2 imitate the situation in Fig.1, the short-circuit point is point A, the breaker T_1 trips fault after several milliseconds (ms), which is similar the operation by thermal trip. It realizes the time-limited fault. When the short circuit point is point B, the breaker T_2 trips, which is also no mores delay time to recovery fault, and it realizes the instantaneous fault.

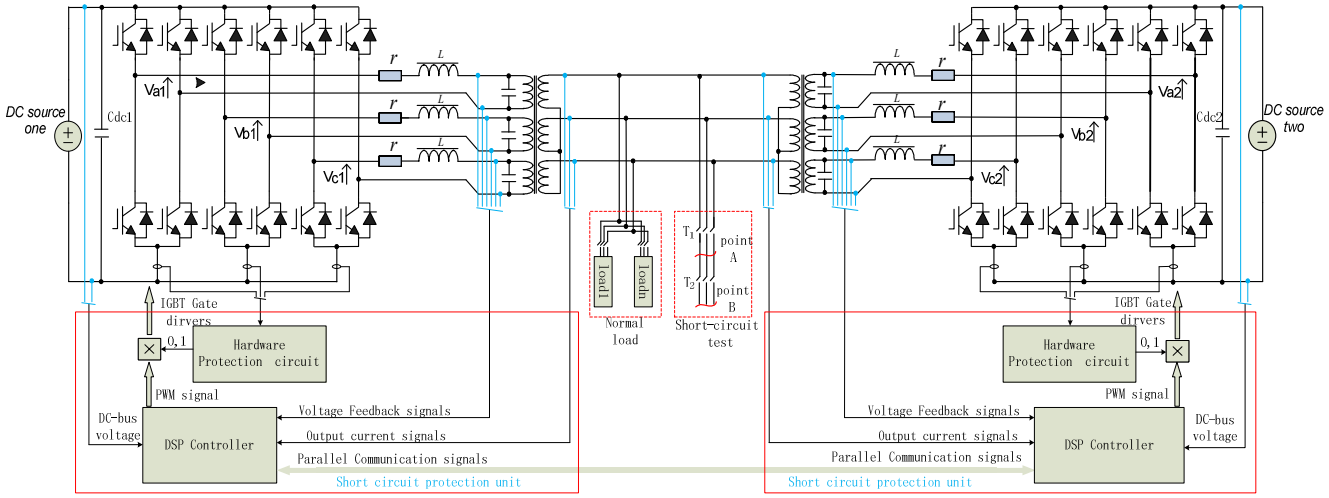


Fig. 1 parallel system based on two combined three-phase inverter

III. Proposed Fault Protection Strategy for Parallel Inverters

Fig.2 shows the proposed five-stage protection operation from the normal state to the recovery state. The inverter is controlled in voltage controlled mode, which supplies the constant voltage for all loads.

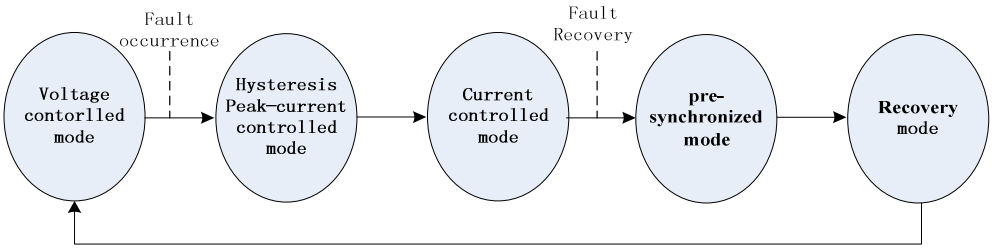
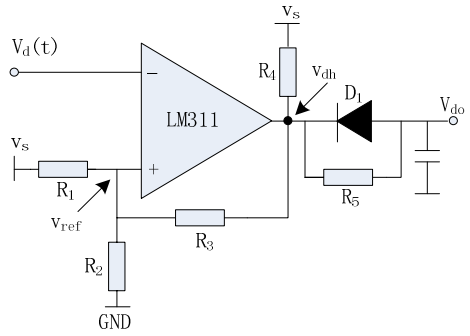


Fig.2 proposed fault protection states

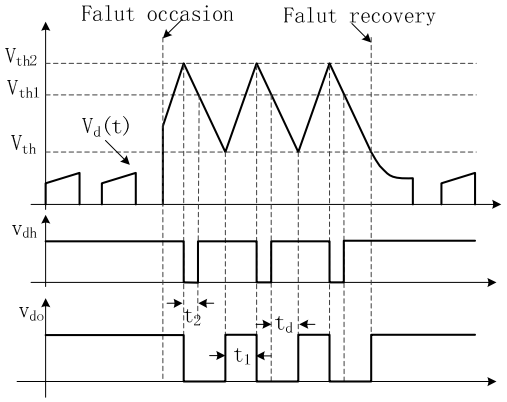
In the normal operation, three-phase inverter is controlled in VCM as a constant ac voltage; PI control can effectively follow the reference voltage without steady state error because it is worked based on synchronous rotating reference frame (dq) [14]. Once short circuit happens at load side, the output current increased largely as load impedance is very small. To protect the switching devices, the system enters into CCM to keep the current within reasonable scope. There is a state transition from VCM to CCM. Ideally, the transition is very fast and smooth. However, a series delay time, such the current sensing delay, calculation time, and digital controlled delay time, results in the fault current, which might damage the switching devices during the interval of the mode transition.

The breaker clears the fault point. The output voltage increases and meets the requirement reference voltage as the output load impedance increased at constant current operation for only one inverter system. However, the parallel inverters system, There are a surge current when the switching time is different from CCM to VCM. Furthermore, the system will be damaged as the large circulated current of each inverter, which reduces the system reliability.

The hysteresis current state is based on the hardware circuit as shown in Fig.3 [10-11]. For the simple explanation, it is assumed that is phase a. The similar analysis and circuit is implemented in other phases. A hysteresis comparator is constituted in Fig.3 (a).The variable Vd (t) is the measured voltage value of dc-link current in phase a. Vs is the source voltage. Several resistors, such as R1, R2, R3, R4, and R5 are designed to meet two different threshold values. Fig.3 (b) shows the key waveform, the peak current is limited with in threshold current by hardware circuit.



(a) Hysteresis



(b) key waveform

Fig.3 Hysteresis comparator circuit and key waveform

The threshold values are expressed as (1)

$$\begin{cases} V_{th1} = \dfrac{R_2 // R_3}{R_1 + R_2 // R_3} V_s \\ V_{th2} = \left(\dfrac{R_1 // R_2}{R_1 // R_2 + R_3 + R_4} + \dfrac{R_2 // (R_3 + R_4)}{R_1 + R_2 // (R_3 + R_4)}\right) V_s \end{cases} \quad (1)$$

Fig.4 shows five-stage structure of two parallel inverters. In normal operation, S_1 and S_2 is zero. Thus, the system is working in voltage controlled mode. Once

short circuit fault happens, the mode is changed from voltage controlled mode to current controlled mode. At first, the hysteresis peak-current mode makes a function to limit the peak-current value as hardware circuit's response. And then the current loop is working to keep the output current constant under S_1=0, S_2=1.

Once short circuit fault is cleared, the system is switched into the pre-synchronized mode. And then the system transited from current controlled mode to voltage controlled mode at the same time for all parallel inverters. To verify the feasible of proposed method, the experiment will be done in next section

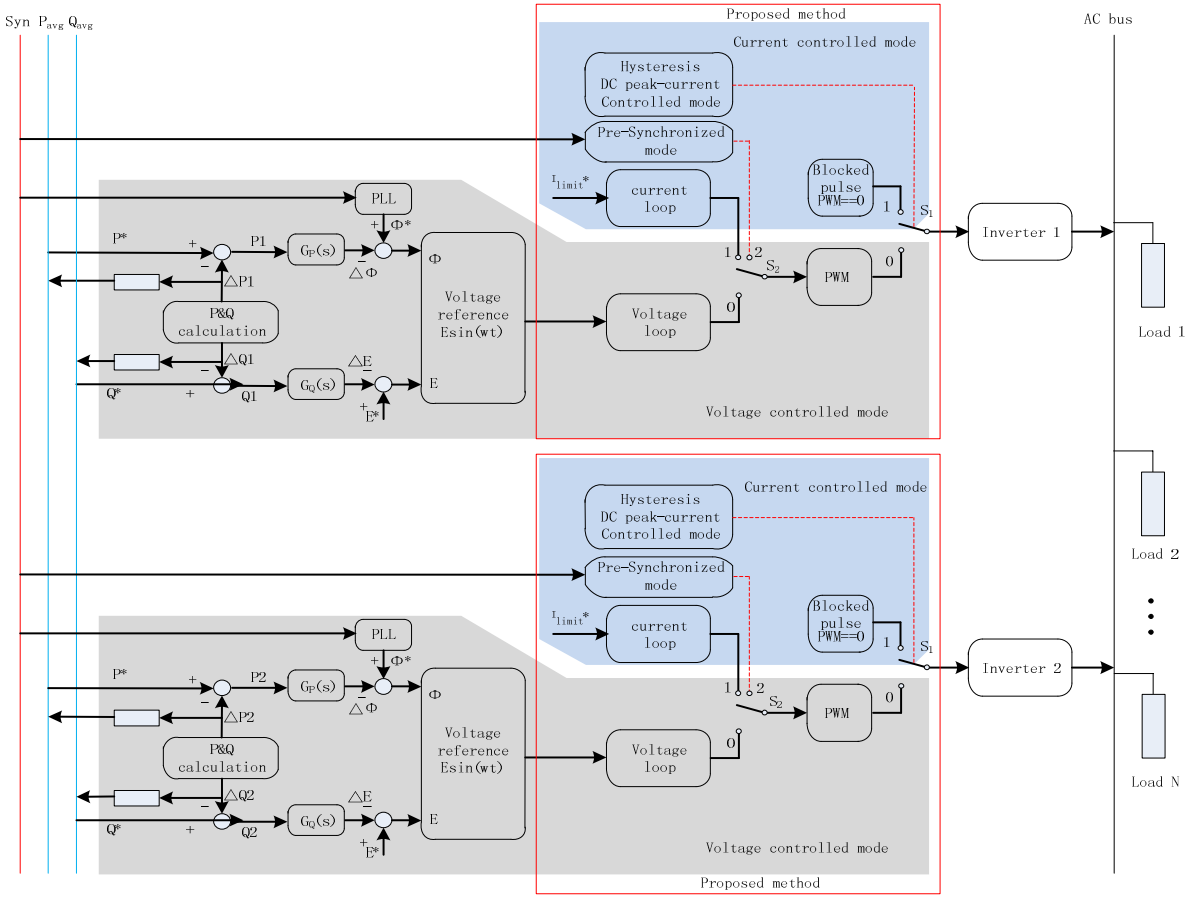
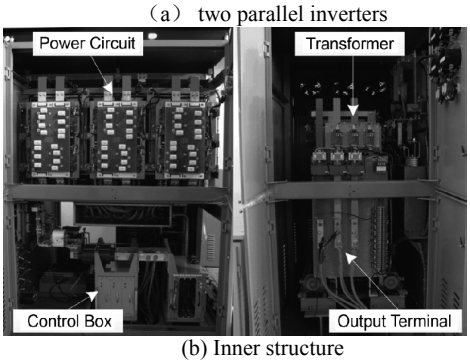


Fig.4 five-stage control and transition structure for parallel inverters

IV. Experiment Results

The parallel system prototypes based on two inverters is built to verify the proposed method. Fig.5 shows the parallel inverters and inner structure.

（a） two parallel inverters



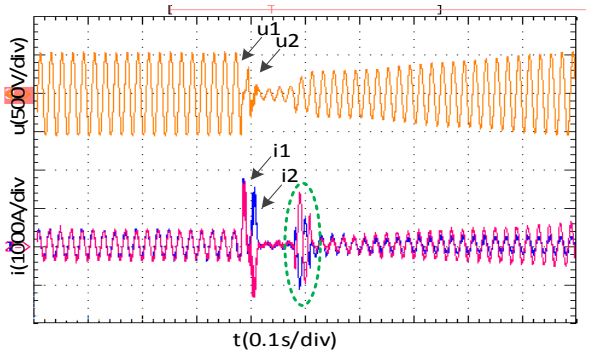
(b) Inner structure

Fig.5 2*400KVA parallel inverters prototype

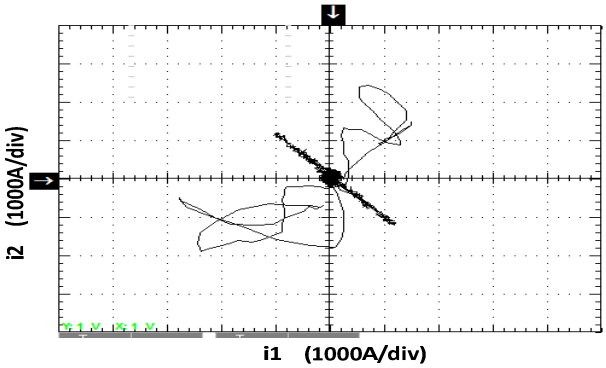
Tab.1 shows the element parameters. The output currents are limited within 2400A due to the hysteresis current state. Fig.6 shows the conventional protection method without pre-synchronized mode. Fig.6 (a), (c) show the experiment waveforms under instantaneous fault or time-limited fault. There are large circulated current when the fault is cleared. Fig.6 (b), (d) shows the difference of two current, there are large scope at second or fourth quadrant, which means the instantaneous currents have an opposite direction.

Tab.1 experiment parameter

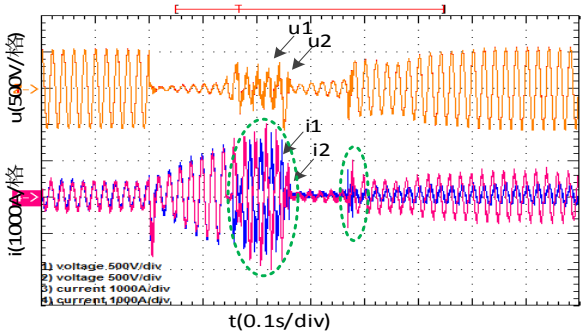
IGBT	FZ2400R17KF6C_B2
Cdc	20000uF
r	0.01Ω
L	60uH
C	2400uF
K	1:1
L_{1k1}	30uH
L_{1k2}	30uH



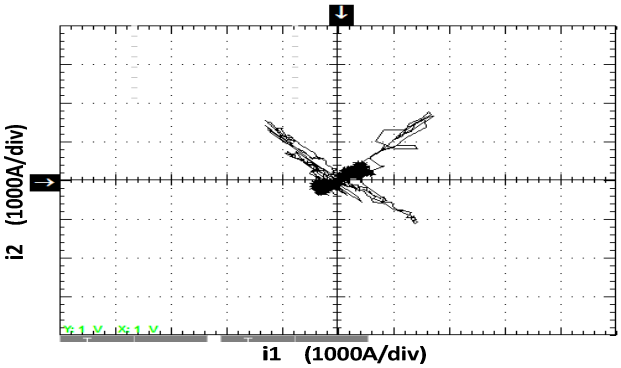
（a） Experiment waveform under instantaneous fault



（b） Difference of two currents under instantaneous fault



（c） Experiment waveform under time-limited fault



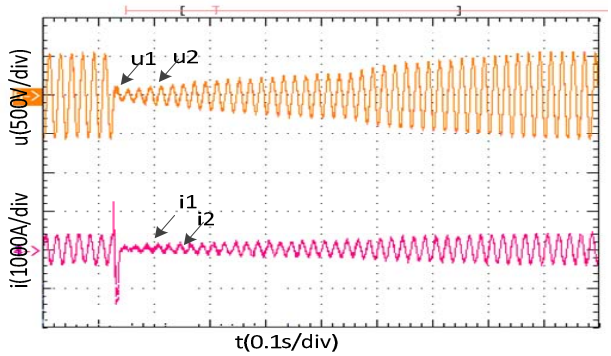
（d） Difference of two currents under time-limited fault

Fig.6 the experiment results of conventional method for parallel inverters

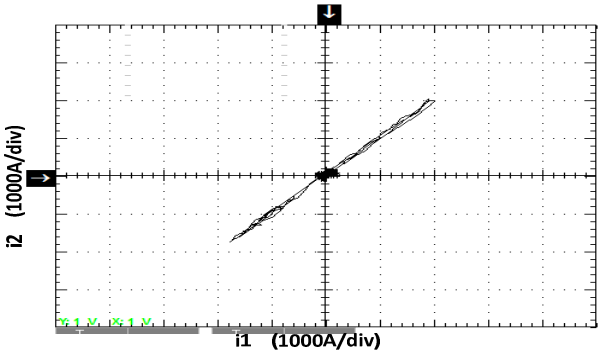
Ch1: Output voltage Vab of inverter one; Ch2:Output voltage vab of inverter two; Ch3:Output current ia of inverter one; Ch4: Output current ia of inverter two

Fig.7 shows the proposed protection method including pre-synchronized mode. Fig.6 (a), (c) show the experiment waveform under instantaneous fault or time-limited fault. They are almost the same at total time. Fig.7 (b), (d) shows the difference of two current. Two

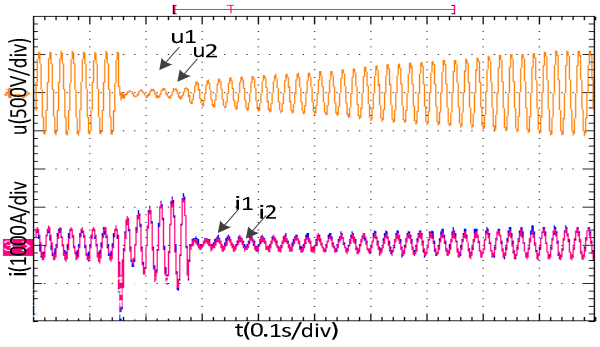
current of inverters are been shared at any time whatever normal operation or fault operation. Compared with Fig.6 and Fig.7, The proposed method can achieve current sharing at steady state operation and limit the surge current at transition operation for parallel inverters. It enhances the system's reliability.



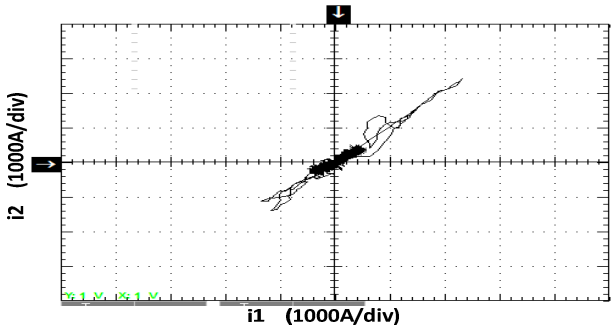
（a）Experiment waveform under instantaneous fault



（b）Difference of two currents under instantaneous fault



（c）Experiment waveform under time-limited fault



（d）Difference of two currents under time-limited fault

Fig.7 the experiment results of proposed method for parallel inverters

Ch1: Output voltage Vab of inverter one; Ch2: Output voltage vab of inverter two Ch3:Output current ia of inverter one; Ch4: Output current ia of inverter two

V. CONCLUSION

A five-stage short-circuit fault protection strategy is proposed for parallel system of high-power three-phase inverters. The output current is quickly limited to reasonable value based on hardware current limiting circuit and software current limiting method. After the fault point is cleared. A pre-synchronized state is provided to keep the synchronized time and then go back to voltage controlled mode, which prevents the surge current from CCM to VCM of each inverter individual. 2*400KVA inverter experiment results shows that the surge current is cancelled by the proposed method. And the output current is shared at any steady-state time and transition time. The system has an excellent reliability to work short circuit fault.

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